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(19)(CA) **CANADIAN PATENT** (12)

(54) Serial Data Interface

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(30) (DE) Germany (Federal Republic of) P 38 29 454.0 1988/08/31

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Abstract of the Disclosure

An interface circuit, for providing data from a data bus to one of a plurality of peripheral circuits coupled to said data bus, examines the bit length of respective datawords provided to the data bus. Only if the bit length of a particular dataword matches a bit length programmed into the interface, will the dataword be coupled to the peripheral circuit. Provision is also made to detect minimal address codes which may be appended to the datawords.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A serial data interface for the connection of a known data bus to a peripheral circuit, wherein a plurality of peripheral circuits are connected to a corresponding plurality of data interfaces and the data bus includes a data line, an enable line and a clock pulse line, characterised by:

- a data store connected to the data line for the successive storage of data words of equal or different word lengths transmitted over the data line;
- a comparison circuit, which detects addresses for peripheral circuits that are possibly present in the data words and compares them with the address of the currently connected peripheral circuit, connected to the data store;
- a control circuit, which compares the word lengths of the data words with a predefined word length and then, taking into account the signals transmitted on the enable line, only allows a further transfer of the data words to the connected peripheral circuit if the two word lengths are equal, connected to the comparison circuit;
- an internal clock pulse generator, which supplies the data store, the comparison circuit and the control circuit with clock pulse signals, connected to the enable line and to the clock pulse line;
- an internal set/reset circuit connected to the enable line and to the clock pulse line, whose outputs are connected to set and/or reset inputs of the data store, the comparison circuit and the control circuit and emits to these outputs corresponding set and/or reset commands which are generated either by an external reset signal or by means of a combination of signals transmitted on the enable line and on the clock pulse line.

2. A data interface in accordance with claim 1, characterised in that, the data store comprises a shift register having n storage cells wherein the number n corresponds to the

number of the bits of the data word associated with the peripheral circuit.

3. A data interface in accordance with claim 2, characterised in that the data store can be placed by the set/reset circuit into a state in which the first storage cell as seen from the input is a logical 1 and the remaining storage cells are logical 0 or vice versa.

4. A data interface in accordance with claim 2 or 3, characterised in that the last storage cells of the data store as seen from the input are components of the comparison circuit, wherein the comparison circuit also comprises a comparison logic to which the outputs of the last storage cells on the one hand and outputs of a module containing the address of the peripheral circuit on the other hand are connected.

5. A data interface in accordance with claim 2 or 3, characterised in that the control circuit is formed as a shift register having a plurality of storage cells, wherein the storage cells are connected to each other via logical combinatorial elements, that outputs of the comparison circuit and of the set/reset circuit are connected to the inputs of the combinatorial logic elements and that a store transfer signal LATCH and a write/read signal WRITE are derivable at outputs of the control circuit.

6. A data interface in accordance with claim 5, characterised in that the control circuit is settable by the set/reset circuit into a state in which the first storage cell as seen from the input is a logical 1 and the remaining storage cells are logical 0 or vice versa.

7. A data interface in accordance with claim 5 or 6, characterised in that the output carrying the write/read signal WRITE of the control circuit is connected to a control logic of

the comparison circuit by means of which the storage cells of the comparison circuit in the writing mode can be connected up as a counter and that a counter output is connected to one of the combinatorial logic elements between the storage cells of the control circuit.

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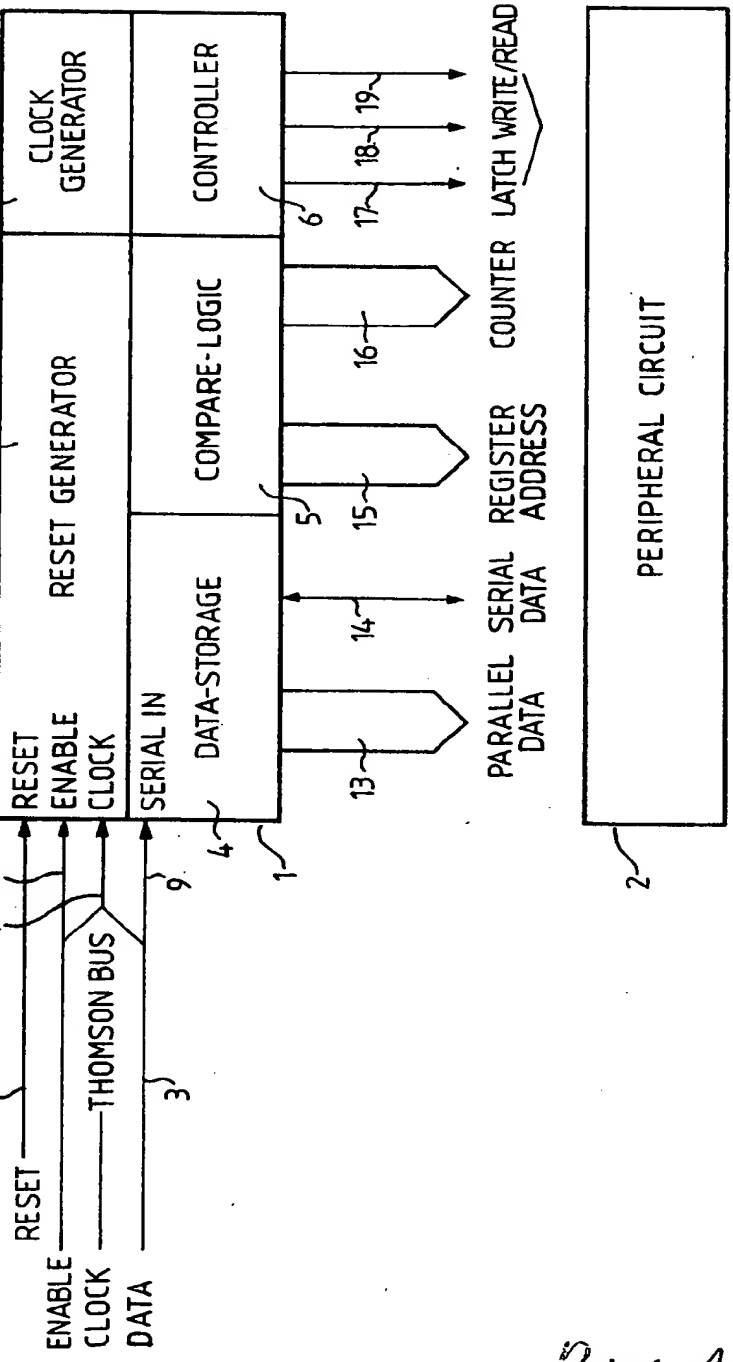
FIG.1



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H 88/052 -1

1328929

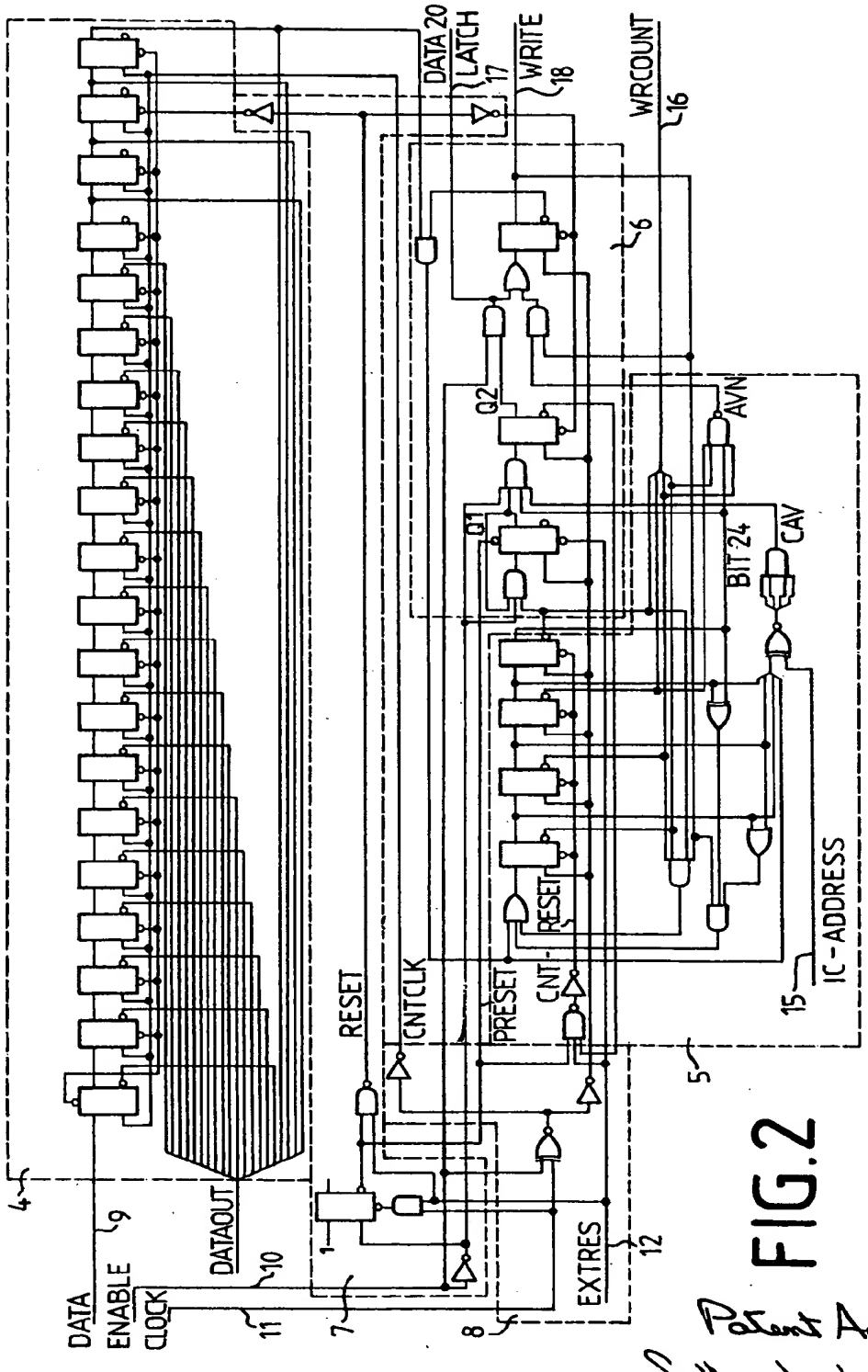

FIG.2

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H 88/052 -2

1328929

FIG.3

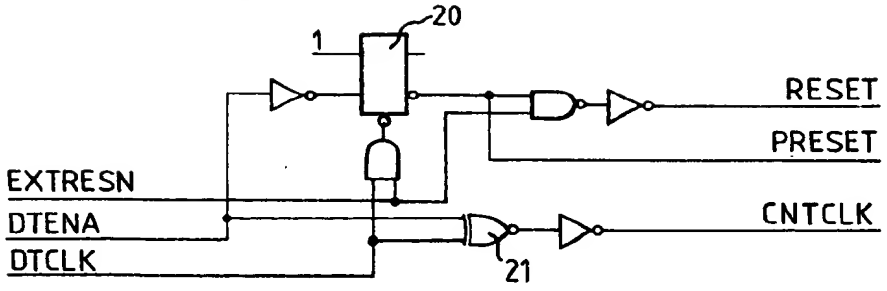


FIG.4

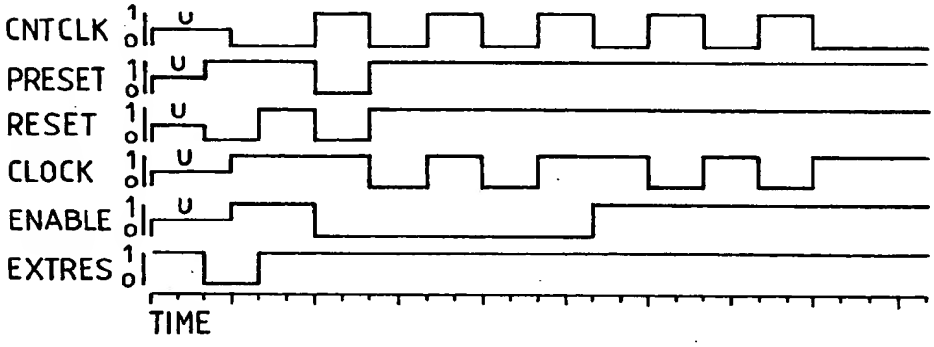
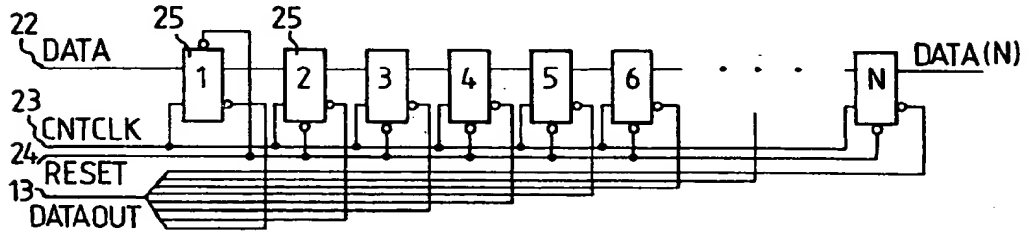


FIG.5



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H 88/052-3

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FIG.6

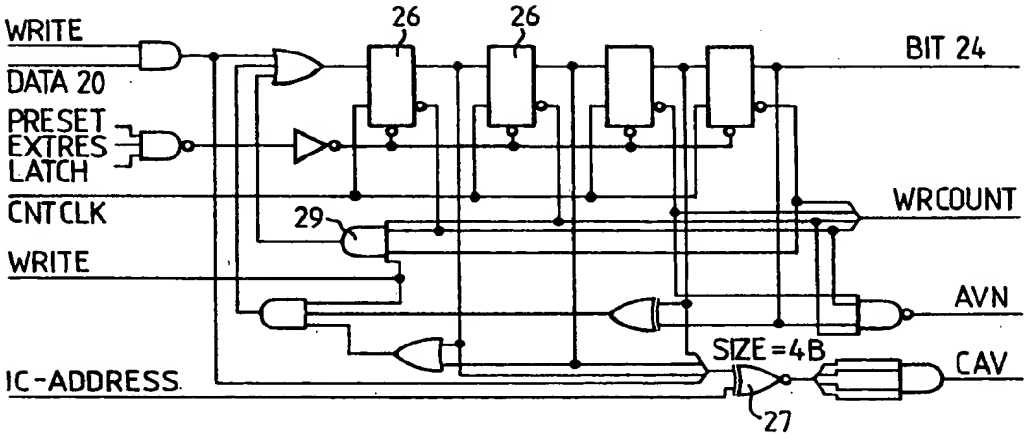
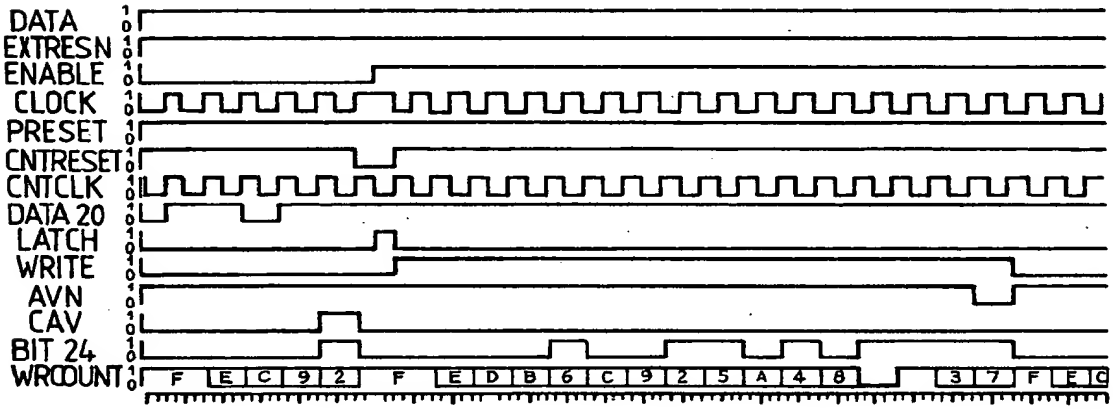


FIG.7



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H 88/052 - 4

1328929

FIG.8

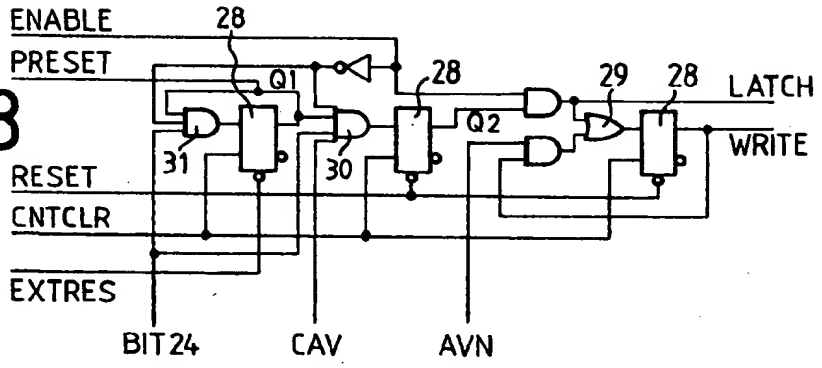


FIG.9

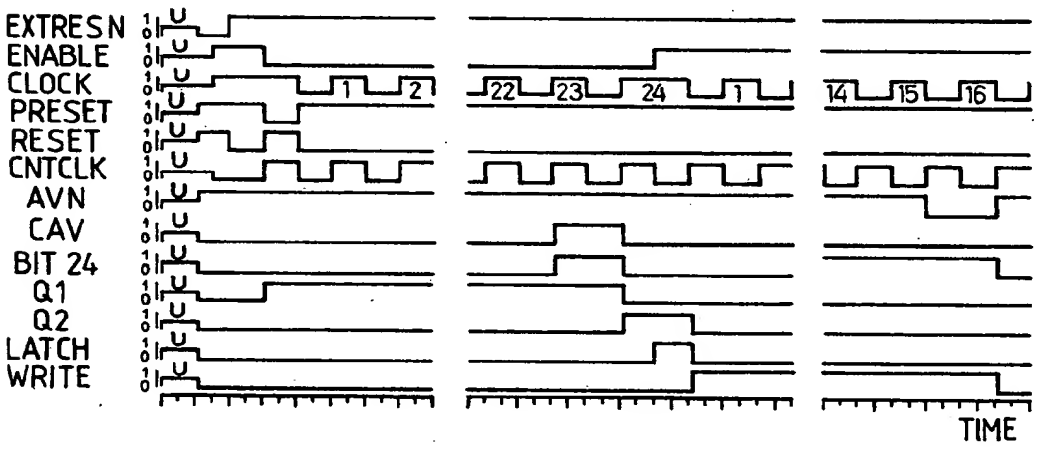
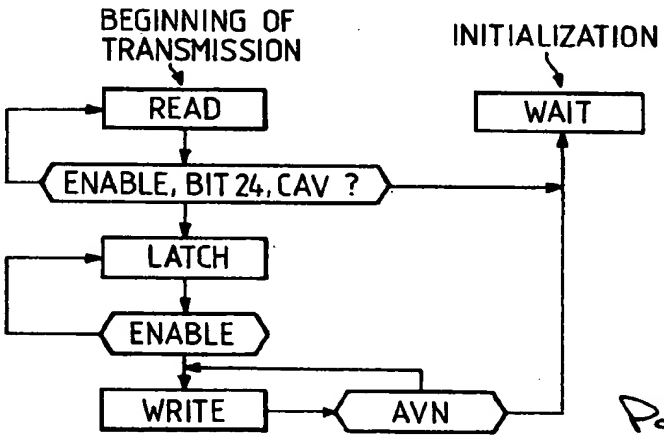


FIG.10



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H 88/052 - 5